Chips to Start-ups Programme Strengthens India’s Semiconductor Design Ecosystem and Industry Ready Talent

Over 68,000 Students Trained and 254 Chip Designs Successfully Taped Out Under C2S Programme

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Guided by the vision of the Hon'ble Prime Minister Shri Narendra Modi to make India a global hub for semiconductor chip design, the Government has undertaken focused policy interventions and sustained investments in semiconductor education, research, and design infrastructure, thereby strengthening the country's semiconductor design ecosystem and talent base.

Chips to Start-ups (C2S) Programme has been initiated for capacity-building across the country and to address the issue of workforce talent gap and chip design infrastructure in the semiconductor design area. C2S Programme aims to generate 85,000 numbers of industry-ready manpower at B.Tech, M.Tech, and PhD levels specialized in semiconductor chip design area.

Under the C2S Programme:

i. More than **68,000 students** have been trained under the programme so far.

ii. Access to advanced Electronic Design Automation (EDA) tools from Synopsys, Cadence, Siemens EDA, Ansys, Keysight, Silvaco, Renesas-Altium, AMD-Xilinx, AsterQuanta, Compcarta, Cadre and AMD-Xilinx has been provided to 332 academic institutions across the country.

iii. Participating institutions have successfully taped out 254 chip designs, comprising 175 designs at the 180 nm technology node at SCL, Mohali, and 79 designs at overseas semiconductor foundries.

In the State of Andhra Pradesh:

(i) 23 academic institutions have been provided access to advanced EDA tools under the C2S Programme,

with cumulative utilization exceeding 4.34 lakh tool-hours as per list given below:

Sr No	Name of Institution
1	Indian Institute of Technology Tirupati
2	Indian Institute of Information Technology Design and Manufacturing Kurnool
3	National Institute of Technology Andhra Pradesh
4	Shri Vishnu Engineering College for Women, Bhimavaram
5	Vignan's Foundation for Science Technology and Research, Guntur
6	Vellore Institute of Technology (VIT-AP) University, Amaravati, AP
7	SRM University, AP
8	Jawaharlal Nehru Technological University (JNTU), Kakinada
9	Jawaharlal Nehru Technological University (JNTU), Anantapur
10	V.R. Siddhartha Engineering College, Vijayawada
11	Anil Neerukonda Institute of Technology & Sciences (ANITS), Visakhapatnam
12	Vishnu Institute of Technology, AP
13	Sagi Rama Krishnam Raju (SRKR) Engineering College, Andhra Pradesh
14	GMR Institute of Technology (GMRIT), Andhra Pradesh
15	G. Pullaiah College of Engineering and Technology, Kurnool

16	Koneru Lakshmaiah Education Foundation, Guntur
17	Vignan's Institute of Information Technology, Visakhapatnam
18	Mohan Babu University, Tirupati, Andhra Pradesh
19	Narayana Engineering College, Gudur, Andhra Pradesh
20	Sri Vasavi Engineering College, Tadepalligudem, Andhra Pradesh
21	Gayatri Vidya Parishad College of Engineering, Visakhapatnam
22	Santhiram Engineering College, Nandyal, Kurnool
23	National Institute of Electronics and Information Technology Tirupati

(ii) The following research projects have been financially supported to promote semiconductor chip design research and strengthen capacity building across four academic institutions:

a) **Development of a secure RISC-V processor for cryptographic applications** – Indian Institute of Technology (IIT) Tirupati.

b) **Development of a hardware accelerator to improve computing performance for high-performance computing and cyber-physical systems** – Indian Institute of Information Technology Design and Manufacturing (IIITDM) Kurnool.

c) **Development of an energy-efficient neuromorphic processor for edge Internet of Things (IoT) applications** – National Institute of Technology (NIT) Andhra Pradesh.

d) **Development of a memory-efficient co-processing unit for edge Artificial Intelligence (AI) applications** – Shri Vishnu Engineering College for Women, Bhimavaram.

The projects are currently at various stages of design and development. Depending on their scope and maturity, they are expected to progress towards prototype validation, including tape-out at semiconductor foundries, wherever applicable.

This information was given by Union Minister of State for Electronics and IT Shri Jitin Prasada in Lok Sabha on 12.08.2026

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