Grant Challenge

India Innovation Centre for Graphene, Kochi

India Innovation Centre for Graphene [IICG] announces Grant Challenges for **Next-Generation Electronics, Communication and Sensors Technologies.**

1. Background

India Innovation Centre for Graphene (IICG), is a pioneering initiative of Ministry of Electronics and Information Technology, Government of India and Government of Kerala along with Centre for Materials for Electronics Technology, Thrissur (C-MET), Digital University Kerala (DUK) in Trivandrum, and Tata Steel Limited (TSL) as the implementation agencies and Maker Village & Kerala Startup Mission as the supporting partners. The application domains of the IICG will be developed with the support of industry partners, including startups at Maker Village, and within the Kerala Startup Mission ecosystem.

2. Aim

To conduct the IICG Grant Challenge which will produce accelerated output for the research topic "**Next-Generation Electronics, Communication and Sensors Technologies**". The winning participants will be incubated as startups in IICG.

3. Grant Challenge Statement

Broad Area : Next-Generation Electronics, Communication and Sensors Technologies

Problem Statement 1:

Title: Design for Graphene based Omnidirectional Radiation Arrays for Sub-6GHz Antenna Application

Introduction:
C-MET, through IICG, is developing graphene-based antennas for 5G and 6G communications. This challenge aims to design and develop graphene based omnidirectional antenna for sub-6GHz applications. The grant challenge will involve design, analysis and optimization of graphene antenna.

Challenge Objectives:

Design, analysis and optimization of graphene antenna:

- **Antenna Type:** Integrated omni directional antenna
- **Operating Frequency Band:** 5 GHz (5150–5875 MHz)
- **Antenna Gain:** 7.5 dBi or more
- **Horizontal Radiation Pattern:** 360° omni directional
- **Polarization:** Dual linear polarization
- **MIMO Configuration:** 2×2 MIMO or any suitable configuration
- **Range:** More than 1 km
- **Wireless Data transfer rate**: 6MBits/s & MCS0 - Tx: 30, Rx: -96, 54MBits/s - Tx: 27, Rx: -81

These specifications are mainly meant for the antenna configuration intended for general area coverage. The proposals are expected with upgraded antenna specifications (such as higher antenna gain, better radiation characteristics, or antenna type) to increase the operational range and improve link reliability, based on various deployment conditions and system-level requirements.

Participants need to submit ideas, designs, product plans, or prototypes of their proposed solutions. The proposer should validate the antenna design through working prototypes. At least 6 numbers of prototypes should be provided as deliverables. The proposer should closely work with C-MET for developing the antenna prototype and testing. C-MET/IICG, at its discretion, will do the field trials with any of IICG/C-MET's partners for validating the prototypes.

Time lines and milestones with predefined deliverables and targeted Technology Readiness Level (TRL) should be included in the proposal.

Problem Statement 2:

Title: Development of Graphene/2D Material based Advanced Sensors

Introduction:

The grant challenge looks for proposals that involves designing, fabrication, and validation of a scalable, ultra-sensitive, and highly selective 2D material-based sensing platform that overcomes current limitations in cross-sensitivity, ambient degradation, and manufacturing reproducibility for critical applications such as environmental monitoring, health care, industry automation, structural health, IoT, aerospace, robotics etc. The proposals must benchmark performance of the proposed sensors against current state-of-the-art silicon or optical alternatives.

Challenge Objectives:

Development of graphene/2D material based advanced sensors:

- **Material innovation:** Specify the exact 2D material system. Detail the material's synthesis route and how the properties will be tailored to ensure high performance sensors.
- **Sensor Configuration & Integration:** Brief architecture detailing sensor configuration and integration of readout electronics, signal-to-noise ratio optimization, etc.
- **Stability and Reliability:** Technical proof of concept outlining how the device will mitigate degradation or baseline drift over extended operation in different environments
- **Scalability Strategy:** A concrete plan demonstrating how the proposed sensor can be transitioned from lab-scale level to high-throughput, repeatable fabrication for mass production
- **Deliverables and Milestones:** A rigorous project execution framework with predefined deliverables and milestones with targeted Technology Readiness Level (TRL)

Participants need to submit ideas, designs, product plans, or prototypes of their proposed solutions.

Problem Statement 3:

Title: Design, Development and Demonstration of Test Platforms for Integration of 2D Materials for FET Applications

Introduction:
Generally, prototyping 2D material transistors rely on manual, low-yield exfoliation and non-standardized contact engineering. This makes it difficult to accurately assess their reliability, variability, and true performance within a CMOS ecosystem.

The grant challenge invites proposals to design, develop, and demonstrate a reliable test platform, test chip, and integration protocol that enables the scalable deployment and characterization of 2D material-based FETs. The solution must also demonstrate a clear path toward integration and characterization of the 2D material to the test chip/platform for transistor applications.

Challenge Objectives:

Design, development and demonstration of Test Platforms for Integration of 2D Materials for FET applications

- **Standardized Test Chips/Platforms:** Development of a universal test vehicle/die layout to rapidly benchmark the transistor characteristics, contact resistance, and reliability of transferred 2D materials.
- Proposals must define the exact structural stack of the test chip. The details of gate configuration, dielectric integration, probing compatibility etc. need to be specified.

- Advanced Contact Engineering: Scalable methods to achieve ultra-low contact resistance using CMOS-compatible metals and geometries.
- The proposal should demonstrate transistor properties of 2D materials with the test chip/platform and atleast 50 No. of test chip should be provided as deliverables
- The proposer should closely work with C-MET/IICG to ensure that the 2D materials developed at C-MET/IICG can be integrated to the test chip seamlessly.
- The proposal should clearly provide evidence of access to essential equipments (e.g., Cleanroom, Lithography, deposition tools, etc.) to complete the development in stipulated timeline.

Participants need to submit ideas, designs, product plans, or prototypes of their proposed solutions.

Problem Statement 4:

Title: Development of Active Noise Cancellation (ANC) System with Graphene based Flexible Piezo-Transducer Films

Introduction:

Under the India Innovation Centre for Graphene, C-MET has developed graphene-based flexible piezo transducers (with 20 to 40 μm thickness and d_{33} of 20-30 pC/N). These thin, transparent, conformable acoustic transducers offer high sensitivity, mechanical durability, and flexibility, making them ideal for integration into wearable electronics, smart textiles, speaker integrated displays, next-generation audio devices, etc. These can also find potential applications in Active Noise Cancellation (ANC) devices. However, realizing its full potential requires a highly integrated, high-performance ANC system. This grant challenge invites academic institutions, research labs, and startups to design, develop, and integrate electronics hardware interface, adaptive algorithms and all other components required to deliver a complete, low-latency ANC solution.

The specifications and Performance Targets of the challenge

Acoustic Performance

- **Acoustic Bandwidth:** Can target any particular frequency range in **20 Hz to 20 kHz** for specific potential application which should be demonstrated
- **Noise Attenuation Depth:** Peak attenuation ≥ **20 dB**; average attenuation ≥ 15 dB across target bandwidth or 90% reduction in acoustic energy across the specified band width

Electronics & Hardware:

- **Power Consumption**: Very low power consumption, ideally ≤ **15 W** during active processing
- **System Latency**: Ultra-low end-to-end group delay (preferably **20 µs** or better)
- **Form Factor:** Miniature footprint suitable for integration onto flexible or rigid-flex PCBs.

Algorithm

- **Convergence Time:** Rapid adaptation to dynamic noise changes
- **Stability Control:** Active feedback loop protection to prevent acoustic howling/screeching.

Scope of Work

Electronics & Hardware Interface: Graphene piezo transducers possess high source impedance and unique capacitive characteristics. The grantee must design a custom Analog Front-End (AFE) and hardware platform. It should include ultra-low-noise pre-amplifiers with programmable gain and impedance-matching circuitry, Ultra-low-latency, high-resolution ADCs and DACs to minimize phase delay and implement a highly efficient Digital Signal Processor and a suitable power management system to prevent any noise.

Algorithm Framework: The ANC algorithm should be capable of handling non-linear electromechanical response of flexible graphene/piezo transducers. The framework should include robust adaptive algorithms, sub-band adaptive filtering, or simplified machine learning-based estimation optimized for low resource utilization. Real-time online secondary path modeling (SpM) to track acoustic path variations during physical deformation/bending of the transducer also should be included.

Device realisation: The proposal should contain details of electronic design with schematics or block diagrams and details of how ultra-low latency will be achieved at the hardware level. The detailed mathematical approach for the adaptive filter and how non-linearities in the flexible graphene material will be modelled with the strategy to maintain loop stability also should be explained. The project milestones and deliverables at each stage should be clearly defined with targeted TRL. The proposer should closely work with C-MET/IICG for the integration of flexible graphene transducers for demonstration of ANC for a defined application.

Prize Money and funding

- For each problem statement maximum up to **Rs 25 lakhs** and free incubation. Aspirants can apply for multiple problem statements. All the IP in this respect will rest with IICG.
- **Duration of Grant Challenge: Maximum 01 Year**

The proposals need to be submitted as per the format to grantchallenge.iicg@gmail.com

Application link:

https://drive.google.com/file/d/169hL_JI9BOwJ70H1QmX2U4cGPBqViYtm/view?usp=sharing

2. Eligibility Criteria

- The challenge is open for all Indian Academic Institutes / Research Institutes / Start-ups / Entrepreneurs

3. Implementing Agency

- The implementing agency will be the IICG, Kochi.

4. Evaluation Methodology

- **Level 1: Screening** - The proposal will be screened based on its merits.
- **Level 2: Presentation** - Shortlisted candidates will be called for presentation for final selection.

5. Important date to be noticed

- Submission last date: 31st July, 2026
- More information on: https://www.graphenecentre.in, and https://cmet.gov.in/

6. Rule and Guidelines

a. All participants and team have to be eligible (See Eligibility Criteria) to participate.
b. During the Challenge, the Team Leader shall be considered as the Single Point of Contact for all engagements & communication by the IICG. Furthermore, the Team Leader cannot be changed during the course of the Challenge.
c. The Team Leader and Team Members will be required to provide working E-mail IDs and Mobile numbers for the purpose of Registration/ Communication.
d. Teams shall maintain detailed documentation of their Idea, Prototype and Solution at all stages of the Challenge for reference and record purposes.
e. The right to summarily reject any change in team composition is vested with IICG.
f. Any IPR if generated in the Grant Challenge shall be jointly owned by the IICG and the contributing team through a separate MoU as per Indian Laws/ Rules.
g. The solution should not violate/breach/copy any idea/concept/product already copyrighted, patented or existing in this segment of the market. Legal liability of such infringement will be the sole responsibility of the applicant team.
h. Anyone found to be non-compliant of rules and guidelines face the risk of their participation getting cancelled.
i. All documents/ papers etc submitted in relation to the Grant Challenge is non-returnable and shall remain as the property of IICG.

j. The number of teams to be finally selected and incubated or not to be selected at all is at the sole discretion of IICG and no suggestions and disputes will be entertained.
k. For any dispute redress, Secretary (MeitY)'s decision will be the final.
l. The selected teams receiving funding through this challenge have to give their written consent to must be willing to be incubated in the IICG.
m. Previous Grant Challenge winners are not eligible for applying the PRESENT Grant Challenges till the project is over.

Appendix 1

Technology Readiness Levels (TRL)

Technology Readiness Levels (TRL) are a method used to measure and assess the maturity of a particular technology

TRL is based on a scale from 1 to 9 with 9 being the most mature technology.

Leve l	Definition	TRL Description
1	Basic principles observed and reported	Lowest level of technology readiness. Scientific research begins to be translated into applied research and development. Examples might include paper studies of a technology's basic properties.
2	Technology concept and/or application formulated.	Invention begins. Once basic principles are observed, practical applications can be invented. Applications are speculative and there may be no proof or detailed analysis to support the assumptions. Examples are limited to analytic studies.
3	Analytical and experimental critical function and/or characteristic proof of concept.	Active research and development is initiated. This includes analytical studies and laboratory studies to physically validate analytical predictions of separate elements of the technology. Examples include components that are not yet integrated or representative.
4	Component and/or breadboard validation in laboratory environment.	Basic technological components are integrated to establish that they will work together. This is relatively "low fidelity" compared to the eventual system. Examples include the integration of "ad hoc" hardware in the laboratory.

5	Component and/or breadboard validation in relevant environment.	The Fidelity of breadboard technology increases significantly. The basic technological components are integrated with reasonably realistic supporting elements so it can be tested in a simulated environment.
6	System/subsystem model or prototype demonstration in a relevant environment.	A representative model or prototype system, which is well beyond that of TRL 5, is tested in a relevant environment. Represents a major step up in a technology's demonstrated readiness.
7	System prototype demonstration in an operational environment.	Prototype near, or at, planned operational system. Represents a major step up from TRL 6, requiring the demonstration of an actual system prototype in an operational environment such as an aircraft, vehicle, or space.
8	Actual system completed and qualified through test and demonstration.	Technology has been proven to work in its final form and under expected conditions. In almost all cases, this TRL represents the end of true system development. Examples include developmental test and evaluations of the system in its intended weapon system to determine if it meets design specifications.
9	Actual system has proven through successful mission operations.	The actual application of the technology in its final form and under mission conditions, such as those encountered in operational test and evaluation. Examples include using the system under operational mission conditions.

Appendix 2

Commercial Readiness Levels (TRL)

Commercial Readiness Levels (CRL) is a framework for defining the spectrum of commercial maturity, from basic market research to full deployment.

CRL is based on a scale from 1 to 9 with 9 being the most commercial technology.

CRL	Description
1	Knowledge of applications, use-cases, & market constraints is limited and incidental, or has yet to be obtained at all.
2	A cursory familiarity with potential applications, markets, and existing competitive technologies/products exists. Market research is derived primarily from secondary sources. Product ideas based on the new technology may exist, but are speculative and unvalidated.
3	A more developed understanding of potential applications, technology use-cases, market requirements/constraints, and a familiarity with competitive technologies and products allows for initial consideration of the technology as product. One or more "strawman" product hypotheses are created, and may be iteratively refined based on data from further technology and market analysis. Commercialization analysis incorporates a stronger dependence on primary research and considers not only current market realities but also expected future requirements.
4	A primary product hypothesis is identified and refined through additional technology-product-market analysis and discussions with potential customers and/or users. Mapping technology/product attributes against market needs highlights a clear value proposition. A basic cost-performance model is created to support the value proposition and provide initial insight into design trade-offs. Basic competitive analysis is carried out to illustrate unique features and advantages of technology. Potential suppliers, partners, and customers are identified and mapped in an initial value-chain analysis. Any certification or regulatory requirements for product or process are identified.

5	A deep understanding of the target application and market is achieved, and the product is defined. A comprehensive cost-performance model is created to further validate the value proposition and provide a detailed understanding of product design trade-offs. Relationships are established with potential suppliers, partners, and customers, all of whom are now engaged in providing input on market requirements and product definition. A comprehensive competitive analysis is carried out. A basic financial model is built with initial projections for near- and long-term sales, costs, revenue, margins, etc.
6	Market/customer needs and how those translate to product needs are defined and documented (e.g. in market and product requirements documents). Product design optimization is carried out considering detailed market and product requirements, cost/performance trade-offs, manufacturing trade-offs, etc. Partnerships are formed with key stakeholders across the value chain (e.g. suppliers, partners, customers). All certification and regulatory requirements for the product are well understood and appropriate steps for compliance are underway. Financial models continue to be refined.
7	Product design is complete. Supply and customer agreements are in place, and all stakeholders are engaged in product/process qualifications. All necessary certifications and/or regulatory compliance for product and production operations are accommodated. Comprehensive financial models and projections have been built and validated for early stage and late stage production.
8	Customer qualifications are complete, and initial products are manufactured and sold. Commercialization readiness continues to mature to support larger scale production and sales. Assumptions are continually and iteratively validated to accommodate market dynamics.
9	Widespread deployment is achieved.